CLAIMS

1. Method for interleaving, according to an interleaving scheme, an input sequence comprising K≥2 bits into an interleaved sequence, said method including the steps of:
a) storing (41; 51) the input sequence in a first memory means,
b) generating (42; 52) first indices (ia; ra,ca) of N succeeding bits of the interleaved sequence, wherein N is selectable from values in the range of 1,2,…,K,
c) converting (43; 53,55,56), according to an inverse of said interleaving scheme, said first indices into second indices (ib; rb,cb) indicative of the positions where said N succeeding bits of the interleaved sequence are stored in said first memory means when they are stored therein,
d) reading out (44; 54) said N succeeding bits from said positions in said first memory means, thereby generating at least part of said interleaved sequence.

2. Method according to claim 1, wherein
- said first memory means is organized in a matrix form comprising rows and columns,
- said first indices comprise first row indices (ra) and first column indices (ca),
- said second indices comprise second row indices (rb) and second column indices (cb),
and wherein said step of converting includes:
- converting (55) said first row indices (ra) into said second row indices (rb) so that inter-row

permutation operations according to said interleaving scheme are performed when said step of reading out is executed,

- converting (56) said first column indices (ca) into said second column indices (cb) so that intra-row permutation operations according to said interleaving scheme are performed when said step of reading out is executed.

3. Method according to claim 2, wherein said step of converting said first row indices includes:

- storing at least one permutation pattern defining said inter-row permutation operations in a second memory means,

- addressing said second memory means with addresses depending on at least said first row indices, thereby causing said second memory means to output said second row indices.

4. Method according to claim 2 or 3, wherein said step of converting said first column indices includes:

- converting said first column indices (ca) and said second row indices (rb) into said second column indices (cb) so that intra-row permutation operations depending on a row index are performed when said step of reading out is executed.

5. Method according to claim 4, wherein said step of converting said first column indices includes:

- determining base sequence indices ($Z_{rb}(ca)$) depending on said first column indices (ca) and said second row indices (rb) by adding index increments (k_{rb})

depending on said second row indices (rb) to previously determined base sequence indices ($Z_{rb}(ca-1)$),
- determining said second column indices (cb) on the basis of at least said first column indices (ca) and said base sequence indices ($Z_{rb}(ca)$).

6. Method according to claim 5, wherein said step of converting includes:
- storing at least said index increments (k_{rb}) in a third memory means,
- storing at least one base sequence specified by said interleaving scheme in a fourth memory means, wherein
- said step of determining base sequence indices is adapted to address said third memory means so as to read therefrom said index increments (k_{rb}),
- said step of determining said second column indices is adapted to address said fourth memory means so as to read therefrom corresponding values of said at least one base sequence.

7. Method according to one of the claims 1 to 6, wherein N is selected to have a value of K, and wherein said first memory means is adapted to generate said interleaved sequence when said N succeeding bits are read out from said positions.

8. Method according to one of the claims 1 to 6, wherein N is selected to have a value of essentially K/M with $M \geq 2$ denoting a sub-sampling factor, and wherein said first memory means is adapted to generate an output sequence representing one of M polyphases of

said interleaved sequence when said N succeeding bits are read out from said positions.

9. Method according to one of the claims 1 to 8, wherein said steps of generating and converting are executed, at least partially, before said step of storing.

10. A computer program product directly loadable into the internal memory of a communication unit, comprising software code portions for performing the steps of one of the claims 1 to 9, when the product is run on a processor of the communication unit.

11. Interleaving unit (60; 70; 80-1,...,80-M) for interleaving, according to an interleaving scheme, an input sequence comprising K≥2 bits into an interleaved sequence, including:
a) an index generator (61; 71) for generating first indices (ia; ra,ca) of N succeeding bits of the interleaved sequence, wherein N is selectable from values in the range of 1,2,...,K,
b) an index conversion unit (62; 72,74,75) connected to said index generator for converting, according to an inverse of said interleaving scheme, said first indices into second indices (ib; rb,cb) indicative of the positions where said N succeeding bits of the interleaved sequence are stored in a first memory means (63; 73) when they are stored therein;
c) first memory means (63; 73) connected to said index conversion unit, wherein said first memory means is adapted to store said input sequence and to generate at least part of said interleaved sequence

when said N succeeding bits are read out from said positions.

12. Interleaving unit (70; 80-1,...,80-M) according to claim 11, wherein
- said first memory means is organized in a matrix form comprising rows and columns,
- said first indices comprise first row indices (ra) and first column indices (ca),
- said second indices comprise second row indices (rb) and second column indices (cb),
and wherein said index conversion unit includes:
- a row index conversion unit (74; 90,91,92) for converting said first row indices (ra) into said second row indices (rb) so that inter-row permutation operations according to said interleaving scheme are performed when said N succeeding bits are read out from said positions in said first memory means,
- a column index conversion unit (75; 100-104) for converting said first column indices (ca) into said second column indices (cb) so that intra-row permutation operations according to said interleaving scheme are performed when said N succeeding bits are read out from said positions in said first memory means.

13. Interleaving unit according to claim 12, including:
- second memory means (92) for storing at least one permutation pattern defining said inter-row permutation operations,
wherein said row index conversion unit includes:
- addressing means (91) for addressing said second

memory means with addresses depending on at least said first row indices, thereby causing said second memory means to output said second row indices.

14. Interleaving unit according to claim 12 or 13, wherein said column index conversion unit includes:
- means for converting said first column indices (ca) and said second row indices (rb) into said second column indices (cb) so that intra-row permutation operations depending on a row index are performed when said N succeeding bits are read out from said positions in said first memory means.

15. Interleaving unit according to claim 14, wherein said column index conversion unit includes:
- first processing means (101) for determining base sequence indices ($Z_{rb}(ca)$) depending on said first column indices (ca) and said second row indices (rb) by adding index increments (k_{rb}) depending on said second row indices (rb) to previous base sequence indices ($Z_{rb}(ca-1)$),
- second processing means (102), connected to said first processing means, for determining said second column indices (cb) on the basis of at least said first column indices (ca) and said base sequence indices ($Z_{rb}(ca)$) determined by said first processing means.

16. Interleaving unit according to claim 15, including:
- third memory means (103), connected to said first processing means (101), for storing at least said index increments (k_{rb}),

- fourth memory means (104), connected to said second processing means (102), for storing at least one base sequence specified by said interleaving scheme, wherein
- said first processing means (101) is adapted to address said third memory means (103) so as to read therefrom said index increments (k_{rb}),
- said second processing means (102) is adapted to address said fourth memory means (104) so as to read therefrom corresponding values of said at least one base sequence.

17. Interleaving unit according to one of the claims 11 to 16, wherein N is selected to have a value of K, and wherein said first memory means is adapted to generate said interleaved sequence when said N succeeding bits are read out from said positions.

18. Interleaving unit according to one of the claims 11 to 16, wherein N is selected to have a value of essentially K/M with $M \geq 2$ denoting a sub-sampling factor, and wherein said first memory means is adapted to generate an output sequence representing one of M polyphases of said interleaved sequence when said N succeeding bits are read out from said positions.

19. Interleaving apparatus (80) for interleaving, according to an interleaving scheme, an input sequence comprising $K \geq 2$ bits into an interleaved sequence, including:
- $M \geq 2$ interleaving units (80-1, 80-2, ..., 80-M)

according to claim 18, each adapted to receive said input sequence and to generate an output sequence representing a different one of said M polyphases,

- a combiner (81) connected to said M interleaving units for combining the output sequences generated by said M interleaving units into said interleaved sequence,

- a control unit (82) for controlling the operations of said M interleaving units and said combiner.

20. Interleaving apparatus according to claim 19, including:

- fifth memory means, connected to said M interleaving units, for storing at least one of a complete set of base sequences according to the interleaving scheme and a complete set of base sequence index increments (k_{rb}).